Atomically Precise, No Interface, Device Regime Workshop

Date: June 7-8, 2012

Locations: The Mansion on O Street, 2020 O Street NW, Washington DC
National Institute of Standards and Technology, Gaithersburg, MD

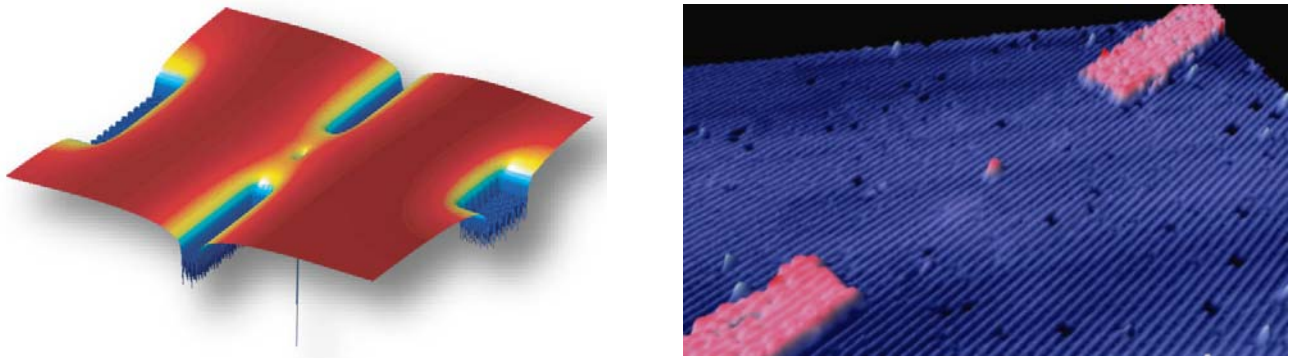
Sponsors: Atomically Precise Manufacturing Consortium, NIST, and Zyvex Labs

Organizers: Richard M. Silver – NIST, ShaChelle Manning – APMC and
John N. Randall – Zyvex Labs

Participants: There were approximately 40 participants from 15 institutions from Australia, Canada, the U.K. and the U.S.

Purpose: To explore the possibilities for novel devices and devices with improved performance in the evolving device regime being explored by the seminal work of Michelle Simmons [1-15] and others. This new device regime creates metallic conductor, semiconductor, and insulator regions by deterministic and atomic precision placement of dopant atoms in Si[1], without metal-oxide-semiconductor interfaces.

Single electron[2], quantum dot[3], and single atom transistors[4], as well as 4 atom wide nanowires[5], and extremely low noise operation[6] have already been demonstrated. The intention of the workshop was to gather some of the world's leading device and atomic precision fabrication experts to explore new possibilities in the quantum computing, digital, and analog device areas and the improvements and extensions of atomic resolution processes, fabrication tools, and modeling/design tools that would be required to enable these new devices.

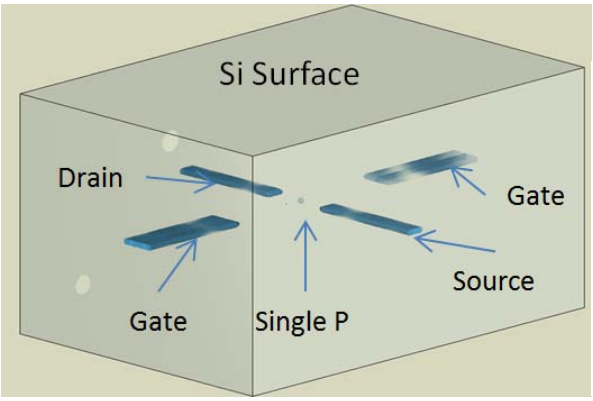


Single Atom Transistor being modeled and fabricated, courtesy of Klimeck and Simmons

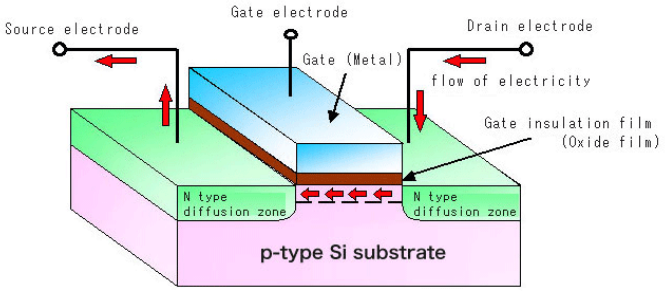
Introduction: Atomically-Precise, No-Interface Device Regime

Recent work at the University of New South Wales in Sydney Australia in the group of Michelle Simmons has shown that it is possible to make transistors in a device regime that is dramatically different than is used for current semiconductor devices.

Using Scanning Tunneling Microscope (STM) lithography and dosing with phosphine, Phosphorous atoms (N-Type Dopants) can be placed by design (both number and position) in the silicon lattice. The device is overgrown with crystalline Si using Molecular Beam Epitaxy and is completely embedded in the silicon. In this way, a number of devices have been made without metal or oxide including a single atom transistor as shown in the figure. In other words this is not a Metal-Oxide-Semiconductor (MOS) device. For comparison, a schematic of a conventional MOSFET device is also shown. The table points to some advantages of this new no-MOS device regime that avoids some of the problems that limit conventional devices.



No-MOS Single Atom Transistor
The Device is well below the surface



Conventional MOS Transistor

Feature	no-MOS	MOS
Free of surface/interface defects	✓	✗
Deterministically placed Dopant atoms	✓	✗
Atomic Precision placement of components	✓	✗
Conduction channel far away from surface	✓	✗
3D circuit architecture possible	✓	✗
Extremely low noise operation	✓	✗
Proven device technology	✗	✓

Executive Summary

The workshop aimed to explore novel electronic, optical and magnetic nanostructured devices. The tools and processes needed and the key challenges faced to realize these devices were discussed. We focused on emerging scanning-probe based approaches that allow atomic precision fabrication and placement of nanosized structures, molecules, and even single atoms in or on Si and Ge. Many other exciting applications of atomically precise fabrication are expected.

The principal conclusions of the workshop are:

- The atomic resolution and precision of STM patterning technology and the lack of heterogeneous materials interfaces for patterns of P dopants in Si have already demonstrated unprecedented advantages to realize components of a quantum computing technology, conducting nanowires, downscaled quantum dot devices, and low noise performance.
- Significant improvements in this technology could be realized by:
    - improving the accuracy and throughput of tip based lithography
    - increasing the variety of species of dopant atoms that can be placed
    - extending the atomic precision placement of dopants to the third dimension.
- Modeling and simulation at the atomic scale on extended device structures is critical for device design, performance optimization, and aspects of metrology.
- Scalable quantum computing may not be obtainable without atomic precision placement.
- Classical digital and analog devices could be improved or developed in this regime.

Classes of devices presently being pursued, and the specific benefits of this technology, include:

- Single P atom Multi Qubit devices (both spin and charge qubits).
    - More control over qubit characteristics through accurate dopant atom placement
    - Expanded design space with 3D electrode placement
    - Better control of individual qubits by screening fields with acceptor dopants
- Resonant tunneling quantum dot devices for digital applications.
    - Improved On/Off ratio through atomically abrupt dopant profiles
    - Deterministic control of electronic states in quantum dots
    - Expanded design space with 3D electrode placement
- Tunnel FET for digital applications
    - Much sharper donor/acceptor profiles leads to superior performance
    - No interface traps or etch-induced line edge roughness

Other areas that would gain advantage from this approach

- Nano magnetic spin devices
    - Magnetic dopants or nanowire inductors for spin control
- Analog RF amplifiers, sense amps, A/D & D/A converters
    - Dramatic reduction in noise would aid analog applications
- Metamaterial Devices
    - Metallic-like nanowires that can be patterned to arbitrary shapes in 3D may offer new avenues for nanoplasmonic and nanophotonic devices.

Given the significant advantages described above, a major effort to research these device possibilities and develop the tools necessary for these studies is highly recommended.

In order to better delineate these advantages, two post-workshop reports will be generated:

1) Scaling Atomically Precise Patterning
2) Modeling Atomically Abrupt P-I-N Junctions

"STM patterning is essential for a variety of quantum devices."

– Rajib Rahman, Sandia National Lab

Workshop Presentation and Breakout sessions

Program June 7:

John Randall, Zyvex Labs	Workshop Goals
Michelle Simmons, UNSW	The No MOS device Regime, Today and Tomorrow
Josh Ballard, Zyvex Labs	Atomically Precise Lithography
Lucian Livadaru, Univ. of Alberta	Silicon Dangling Bond Structures for Nanoscale Devices
Gordie Shaw, NIST	The small force metrology project
Richard Woolley, U of Nottingham	Automated Probe Optimization: A step closer to atomically precise engineering?
Steven Schofield, UCL	Energy States in Dangling Bonds
James Owen, Zyvex Labs	Top Down Meets Bottom Up

Program June 8:

Carl Williams, NIST	Welcome and thoughts about quantum computing
Michelle Simmons, UNSW	Devices made to date in No MOS regime
Gerhard Klimeck , Purdue	Modeling devices in No MOS regime
Rajib Rahman, Sandia	Quantum Device Design with STM Patterned Nanostructures
Richard Silver, NIST	No MOS Nano device possibilities
Frank Register, UT Austin	New devices and integration schemes for atomically precise manufacturing
Malcolm Carroll, Sandia	Semiconductor double quantum dot qubits for adiabatic quantum computing
Ezra Bussman - Sandia	STM fabrication of double quantum dot charge qubits for adiabatic quantum computing
Break out Session 1	Device brain storming
Break out Session 2	Process, tool, and modeling priorities

I. Summary of Workshop Activities

Presentations: The workshop consisted of 15 formal presentations, each followed by significant discussions. Most of the presentations are included in the permanent record of this Workshop along with a synopsis of each presentation. The entire record of the workshop will be made available on the Web by or about July 2012. Many of these presentations included unpublished material and therefore several of these presentations have been abridged to exclude the unpublished results. A few of the presentations were, at the author's request, suppressed entirely.

Breakout Sessions: The workshop also included two breakout sessions. For each breakout session we divided into three groups of roughly the same size. We encouraged participants from the same institution to spread out through the three groups. We also encouraged the three groups to re-form with a different membership for the second breakout session.

For the first breakout session, all three groups were charged with the same mission:

- 'Produce a high-priority list of device ideas that could potentially benefit from fabrication in this new device regime', elect a spokesperson, and have that spokesperson report to all workshop participants their group's finding.

The second break out session was run in a similar manner but with the topic:

- 'Produce a high-priority list of tools and processes that would be necessary to realize the devices identified in the first breakout session.'

The outputs of these breakout sessions from the three different groups have been merged in what is reported in the following pages.

Post workshop reports: Significant interest in several areas prompted several groups to volunteer to do follow up reports. These will be appended to this workshop report when completed by September 2012.

- Scaling Atomically Precise Patterning – Zyvex Labs
- Modeling Atomically Abrupt P-I-N Junctions – Purdue and Sandia

II. Breakout Session 1 - Device Ideas:

The ability to place dopant atoms with atomic precision as developed by the Simmons group, in three dimensions in Si[1-6] and/or Ge[7, 8] has a number of significant advantages for electronic devices that span analog, classical digital information, and quantum information processing devices. The fact that metallic conducting, semiconducting, and insulating regions can be produced with extremely sharp boundaries, in an area that has effectively no material boundaries has a number of significant advantages that may be exploited.

- With no metal oxide semiconductor (MOS) interfaces there are none of the associated defects, charge traps, or interfacial roughness to introduce noise[6] or degrade device performance[2].
- Atomically precise control over the number of dopant atoms and their placement allows unprecedented control of the energy levels in quantized structures (such as quantum dots) and the level of interaction between these quantized energy levels[2-5]. This should lead to more predictable and reliable device performance.
- During the workshop several presenters mentioned some of the limitations of planar architectures when placing control and readout electrodes required for desired operations. The ability to place dopant atoms with atomic precision in three dimensions[9, 10] would avoid many of these limitations.
- Improvements in atomic precision fabrication can be applied to aspects of conventional MOS device architectures, for instance deterministic placement of dopants in channels, or atomically defined volumes of pure Si.

The participants of the workshop identified several classes of electronic devices that could benefit from this new device regime made possible by emerging atomic resolution processing. They are listed below:

A. P in Si Quantum Computing Devices

While there are many routes to quantum computing, the expected level of required redundancy suggests that reasonable levels of integration will be required to produce quantum computing systems that are practical. This demands that quantum computing devices and architectures need to be scalable with respect to the number of qubits in a computing system, and needs to be integrable into a conventional CMOS architecture. For this and many other reasons, the P in Si (and Ge) approach being pursued by the Simmons group appears to be one of the most attractive, as it is supported by existing semiconductor processing technology.

While single ion implantation for placement of individual P dopants has yielded some interesting results, the inevitable uncertainty in position due to limited spatial resolution in position of ion impact and straggle of ion trajectory after implant will simply not support the required precision in placement of the P atoms. Rahman explicitly made this point in his presentation. This leaves H depassivation lithography, phosphine dosing, and epitaxial overgrowth as the consensus approach for building P in Si quantum computing devices. This technique alone is the only one that can place P atoms accurately enough to have them interact effectively as either spin[11] or charge qubits.

B. Atomic Precision Tunneling Field Effect Transistors (TFET)

In his presentation, Frank Register pointed out that TFETs have been identified as a very promising device for future technology nodes, but band tailing effects have limited the performance of these devices. With atomic precision placement of both N and P type dopants giving extremely sharp PN junctions, combined with three dimensional arrangement of gate electrodes, tunnel FETs fabricated[9,12] with these approaches should have superior performance. Klimeck and Rahman concluded that the extremely sharp P-N junctions were something that can be modeled with their simulation software NEMO[16] in a very short period of time. This simulation will be included in one of the post-workshop reports.

C. NO MOS low noise analog amplifiers

Analog devices are far more sensitive to noise than digital devices. The unprecedentedly low noise demonstrated by conduction in ∂-doped P in Si devices[6] points to a major opportunity to develop analog circuitry with much better noise performance leading to enhanced dynamic range. RF amplifiers, telecommunications, low-noise, high-speed, low-power-consumption amplifiers, control circuitry for quantum computers, and analog to digital and digital to analog converters are exciting opportunities. It was proposed that a simple FET type device be created in this regime to test the potential advantages of low noise analog and/or digital devices. Existing modeling/design tools such as NEMO could be used to design such a device. Several participants liked the idea of fabricating STM preamplifiers as a bootstrapping process.

D. Resonant tunneling devices with improved On/Off ratio

Previous versions of resonant tunneling devices and circuits were limited in their on/off current ratios. The greater precision in size control and placement of quantized structures available in this new regime should remove this limitation. The three dimensional placement of device elements should also have significant advantages. Circuit and device approaches previously conceived, but abandoned because of fabrication issues, could be enabled by this technology. For instance a proposal for a complex logic cell based on a resonant tunneling quantum dot architecture that proved impractical because of limitations in materials and fabrication may very well be possible in the No-MOS regime[17].

E. Magnetic impurities

Nano magnetic devices of various sorts including spintronic devices, were of significant interest to several workshop participants. Patterning of an element such as Mn, which is used as a magnetic impurity in III-V semiconductors, and is also ferromagnetic in Si[18] could provide a route to fabrication of such devices.

Giant Magneto Resistance may be more effective if we could reduce the layer thickness and reduce the surface roughness (but this is typically in non-Si systems). A spatial standard for MFM could be developed. Another suggestion was to use three-dimensional placement of atoms to create a spiral inductor that could be used to create a localized and controllable magnetic field.

F. Optical devices

A number of optical devices were deemed to be of interest by taking advantage of the atomic precision size control and/or the inclusion of Er as a dopant (if possible) that could be placed with atomic precision. It was also suggested that short wavelength optical devices might be of significant interest. A plasmonic photodetector device integrated in CMOS, comprising a particular shaped nanoaperture, has already demonstrated increased photocurrents by exploiting plasmonic behaviour[19]. A key advantage of manufacturing with atomic precision would be the integration of optical and electronic components, particularly when exploiting the properties of plasmonic behavior[20]. Not only could the atomically precise fabrication of silicon construct well defined subwavelength waveguides for focusing light, but this can also be coupled with the direct integration of suitable dopants for high sensitivity low loss devices. This could find application in the bio-photonic and telecoms market. Single molecule detection using SERS and possibly TERS[21] (surface and tip-enhanced Raman spectroscopy) could open up the door to nano-bio-photonics and lab on a chip.

G. Dangling bond as quantum dot devices

Both Steven Schofield and Lucian Livadaru described dangling bonds, or depassivated H atoms as quantum dots with discrete energy states. Livadaru described how these quantum dots can be used as elements in a Quantum Cellular Array (QCA) architecture as described by Lent et al.[22] at Notre Dame. The QCA architecture has been shown to be able to form a complete logic architecture. Although significantly different than Simmons's P-in-Si approach this is also a device regime that has no material interfaces, but all activity occurs at the surface of the silicon crystal, so that large atomic terraces would be required for device construction. The advantages of this architecture include extremely low power and extremely small devices.

H. Enhanced crossbar QCA and CMOL architectures

There are some interesting circuit architectures that might benefit significantly from this new device regime. It was postulated that crossbar architectures or Likharev's CMOL architecture[23] might be realized in a much more robust form. Crossbar-like architectures suffer fundamentally in their energy balance from diode-based leakage or dark currents. Atomically precise crossbar links, possibly based on single electron charging, may offer the capability to reduce the unintended current flow. Lent's Quantum Cellular Automata (QCA) architecture[22] in its quantum dot incarnation or magnetic incarnation may also become more realizable in atomically precise manufacturing.

I. Engineered nucleation sites for metal oxide crossbar switches

There are a number of crossbar switch or memory devices that operate by filamentary growth in Metal Oxides. There are device limitations in the variability of this material transformation in part because the unknown nucleation of the filament growth. It was postulated that nucleation sites might be engineered by atomic precision processing and that the result would be more reliable device operation.

J. Single electron pumps

With superior control of dimensions, electronic states, and the control of those electronic states it is suggested that single electron pumps would benefit significantly from this device regime.

K. Si terahertz lasers

Recently proposed[24] THz technology is based on a $2p^0$ to 1s transition in a donor atom in silicon. So far, all the experiments have used a bulk-doped sample in the low doping limit where this energy difference is fixed and only varies slightly from one donor species to another. Since the No-MOS regime enables us to create precise donor islands with controlled doping density (in the high doping regime), covalent interaction between neighboring donors will change the $2p^0$-> 1s gap. It may be possible to engineer this gap precisely, and hence to control the wavelength of the emitted radiation.

L. Medical devices

The emphasis on health care and the wide range of new analytical techniques make this a category that should at least be considered. A small, low-noise, low-power set of electronics perhaps could be developed in the No-MOS regime that would be attractive for implantable medical devices or for ultrasensitive analytical devices. Another possibility is DNA sequencing nanopores. Constructing nanopores for this purpose could involve tip based atomically precise fabrication, and the integrated electrodes and sense amps could be No-MOS devices. It was suggested that an array of nanopores could be deliberately constructed with different size/shape pores to optimize the accuracy of the sequence reading.

M. Strain sensitive devices

No-MOS devices integrated into AFM cantilever might be a good strain gauge, but the discussion did not yield ideas of how this technology might produce a clear advantage.

III. Breakout Session 2 -Process/Tool development priorities:

Atomic precision lithography and dopant placement, low temperature epitaxial overgrowth and other processes that enable this new device regime are all in their infancy. All of these processes have significant room for improvement and some have not yet been developed. With the device concepts enumerated in the earlier breakout sessions, the following tools and processes were discussed and prioritized.

A. Other Substrates

While Si(001) has many advantages, not least being the substrate of choice of the semiconductor industry, the use of other substrates would broaden the applications of this technology. Higher-mobility substrates such as Ge, graphene, GaAs would improve device performance. Silicon on Insulator (SOI) substrates reduce leakage currents into the substrate. A wide bandgap material that could be grown epitaxially on Si would give an alternative to intrinsic Si for an insulating layer, or provide modulation doping of Si. Si(111) and Si(110) were mentioned as other possible Si substrates.

B. Automated SPM

The automated operation of scanning probe microscopes such as demonstrated by Richard Woolley and Zyvex Labs, has a significant opportunity to improve productivity in one of the primary tools for developing devices in this new device regime.

C. Other dopants

An acceptor (group three) dopant would be required for a number of the device applications discussed in the workshop. For example, mixed donor-acceptor doping would provide stronger band bending, and provide deeper donor levels, desirable for higher-temperature device operation. More generally, a process for placing and maintaining the atomic precision placement of dopants including Ga, In, Al, As, Sb, Er, Mn or other magnetic species, NV centers in diamond etc. would widen the range of nano devices that could be produced in the No-MOS regime.

The technology developed by Simmons for P incorporation works well but can still be perfected for one atom accuracy placement. A study of dopant placement, incorporation, activation, and overgrowth that minimizes or eliminates dopant placement uncertainty will be required for all different species incorporated.

D. Other species that deposit selectively

The present focus to phosphorus dope Si is just the tip of the iceberg. Early on the pathway toward process development, literature searches should be done along with exploratory experimental and theoretical work to identify possible species that could be included in the toolbox for atomically precise fabrication. Simmons has produced a book chapter on species compatible with H-resist lithography[13]. While there are many issues to consider, three specific requirements should be the first to consider:

- Bonds to patterned areas
- Doesn't bond to passivated areas
- Can be passivated and unpassivated (to permit Patterned ALE or ALD of 3D structures)

E. More reliable tips

STM tips are the primary tool and sensor used in STM lithography and imaging respectively. They are also notoriously variable, capricious, and a major liability when it comes to instrument productivity. Tip construction, materials, and operation are all key areas to be explored. TipTek[25] a spin off company from Joe Lyding of Univ. Illinois is developing alternative tip materials such as HfB_2 coatings for STM tips.

F. Registration and other processing for 3D patterning

In order to place dopant atoms with atomic precision in three dimensions, a process for aligning to previously written patterns that have been overgrown with one or more layers of epitaxial Si must be developed[14,15]. Either the ability to image previously-buried dopants, or the ability to reference a registration mark which has survived the overgrowth will be required. Obtaining nicely ordered, atomically flat Si surfaces after epitaxial overgrowth[14] would be desirable for this purpose. Methods to obtain such a surface at temperatures compatible with maintaining the atomic placement of dopants will be necessary, for example, ultrafast heating with an IR laser, or patterned epitaxy.

G. Better H depassivation litho

While both Bussmann and Simmons indicated that their current patterning capability is adequate for their research, it is clear that the lithography tools must improve if significant progress is to be made in this area. Specific areas that should be developed include:

- Automated alignment to the Si lattice
- Design tools that use the Si lattice as a pixel grid
- Device design rules
- Automated alignment to registration markers
- Field stitching (accurate course positioning)
- Improved tip technology
- Closed loop nanopositioning of the tip with ~ 0.15nm precision

Additionally the group expressed a desire to see one or more technical paths to scale the throughput and area that an atomically precise lithography tool could address for more advanced research and eventually manufacturing. Some examples discussed include:

- **Multi tip systems**
- Variable spot size patterning modes
- Mix and match with higher throughput patterning such as nanoimprint

This will be followed up in one of the post-workshop reports.

H. Contact technology for No-MOS devices

There is a need to study contacts with the devices. Is the method used by Simmons good enough? Will there be a need to move to other methods of contacting, like low T silicides[26]? If we make super-low noise No-MOS devices, we will require contacts which do not introduce high noise themselves.

I. Better modeling and design tools

While there are some tools, such as NEMO, which have proven valuable in modeling in this device regime, developing the device types that are mentioned above would be aided significantly by improved modeling and design tools. There is a need to bridge from the atomic scale to the mesoscopic scale. Atomic scale methods and classical approaches both work, but they will need integration. This is especially important for surfaces. Beyond CMOS, the design space is just huge, so there is a need for efficient tools for design surveying. NEMO results for P in Si have been validated extensively against other DFT methods[27]. Further work is needed for other impurities / dopants, especially under strained conditions. Full electron flow calculations under non-equilibrium conditions outside the Coulomb-blockade regime have not been performed on these device classes, but would seem to be critically needed to estimate energy losses and heat generation.

Capabilities that would be desirable would include:

- Some design rules for fabricating different classes of devices.
- Ability to predict electrical crosstalk etc.
- Need a model to predict tunneling rates between structures efficiently.
- **Ability to predict coherence lengths, coherence times, and energy losses under experimentally relevant conditions.**
- **Ability to predict current flow under non-Coulomb blockade conditions.**

J. Integration Scheme with CMOS

Carl Williams and Frank Register in their presentations, as well as a number of others in breakout session discussions, brought up the issue of integration of No-MOS devices with CMOS devices. The current high temperature processing in both device regimes makes homogeneous integration processing difficult or impossible. Flip chip or 3D packaging is a possible avenue. Some sort of technical paths should be explored. Several participants see this as a major issue that really requires a dedicated approach.

K. Selective Epitaxy

Selective epitaxial processes such as patterned Atomic Layer Epitaxy[28] (ALE) (being pursued by Zyvex Labs) would have a number of advantages, not the least of which would be in aiding the alignment to previously defined dopant patterns. The patterned ALE process might also permit selective growth to produce better surfaces for subsequent patterning steps.

L. Lower temp processing

The high temperatures required to produce well-ordered Si (100) 2x1 surfaces have multiple drawbacks. Post processing of Si that already contains CMOS circuitry is excluded. Etched alignments marks must be disproportionately large to survive the high temperature processing. A surface preparation process, for example an ex-situ wet chemical etch process, that operated at much lower temperatures and resulted in well-ordered Si (100) 2x1 surfaces would be beneficial.

M. Deal with large screening length in Si

A current limitation in controlling the energy state of individual device elements by electrostatic interaction of gate electrodes is that the screening length of intrinsic Si is relatively long (~100nm) compared to the desired spacing of, for instance, P atoms to make qubits (~20nm). This makes it difficult to isolate the effect of a gate electrode to the intended device component. One potential solution would be to use other dopants (for instance acceptor dopants) that could be strategically placed to screen the effect of the electrode to the intended device component. Three dimensional placement of dopants would improve the ability to do this sort of screening, which would be verified in modeling and subsequent experiments.

N. Other resists

A patterned monolayer of H has proven effective for the selective deposition of P[10], Si[27], and Ge. However, H is not an effective mask for many potentially useful tasks such as high-quality overgrowth, because the H becomes mobile on the Si surface at 300°C and above. There was an interest expressed by several workshop participants to explore other monolayer resists that are also self-developing and could be patterned with atomic precision. Self-assembled monolayer resists are an additional area of interest.

O. H repassivation

One of the advantages of H depassivation lithography is the ability to examine a pattern after it is written for error correction. If there are some H atoms in the pattern which were not successfully removed, then more lithography can be used to remove the unwanted H atoms. However, for H atoms that have been unintentionally removed there is no current process to "repair" the defect by selectively repassivating the Si surface. Such a process would be desirable and work is underway at Nottingham (Moriarty and Woolley)[29] to repassivate, possibly using force mediated chemistry using an SPM tip with a selected structure [see Ref.29 for details on effect of different tip states using dynamic AFM].

P. Large Terraces

Current sample preparation for Si (100) 2x1 surfaces produces surfaces with relatively small atomic terraces (<100nm). Work by Simmons[30] and Silver[31] have used etched features and high temperature annealing to create relatively large atomic terraces as large as 10μm. However, the small terraces and step bunches surrounding the large terraces, and the long periods of high temperature annealing required, are often undesirable. A process that produced large terraces with lower temperature processing would be desirable.

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COMMENTS from participants with respect to this summary:

From ShaChelle Devlin Manning

The importance of the impact of atomically precise manufacturing on the economy should not be underestimated. This is a disruptive technology with the potential for dramatic job growth in both the direct manufacturing arena, the enormous number of novel high value applications that it will create, and the indirect jobs created and ancillary business.

From Tihamer Toth-Fejel

Great summary! You caught all the important points I heard (e.g. error-correction, multi-tips, mix-and-match with nanoimprint,).

Just two things to think about:
1. I heard quite a bit of talk regarding the difficulty of getting perfect tips (that is what Joe Lyding's company is commercializing; better tips). I did hear some talk about using Patterned ALE to try to build better tips. While I have little idea of exactly how this could be done (e.g. different chemistries), I suspect that such bootstrapping would do wonders.
2. On a related issue, I did not hear much about NEMS applications, other than possibly as sensors (nothing about sorting or complex enantiomeric chemistry). In the long term (next project?) the most powerful and high-leverage (but perhaps quite difficult) NEMS goal would be implementing the entire MEMS tip and electronics in a smaller, atomically precise implementation.

From Richard Silver - NIST

While we certainly need to explore other material systems, any deviation from Si 100 will be met by great skepticism from the existing semiconductor industry and have many additional hurdles as a result. I still believe that ultimately, the semiconductor industry will implement most device advances arising out of atomic scale device research. Certainly Intel and others are currently looking at sub-5 nm device architectures right now.